

Remarks/Arguments:

Applicants acknowledge, with appreciation, the opportunity provided to Applicants' representatives (Mssrs. Christopher Spletzer and Jacques Etkowicz) to participate in a telephone interview with the Examiner on March 9, 2005.

Applicants note that the Information Disclosure Statement filed with the application on October 16, 2003 (IDS #1) has yet to be acknowledged. Applicants respectfully request IDS #1 be acknowledged and a copy of the acknowledged 1449 provided to applicants with the next official action.

Claims 1-11 are pending and claims 12-23 have been withdrawn from consideration.

Rejections Under 35 U.S.C. §102

The Office Action at page 2, paragraph 3 sets forth "Claims 1, 2, 3, 7, 9, 10 and 11 are rejected under 35 U.S.C. 102(a) as being anticipated by Shimanuki et al. Japanese Patent Abstract Publication No. 2002-368029." Applicants acknowledge with appreciation the indication that claims 4-6 would be allowable if rewritten in independent form.

Prior to the telephone interview conducted on March 9, 2005, Applicants filed an Information Disclosure Statement on February 22, 2005 disclosing the references cited in an International Search Report in corresponding PCT International Application No. PCT/US2004/018000. These references included (1) U.S. Patent Application Publication 2003/027918, (2) U.S. Patent No. 6,395,807, (3) GB Patent No. 2,279,944 and (4) EP 0601323. During the telephone interview on March 9, 2005, each of references (1)- (3), as well as Shimanuki, were discussed. Further, prior to the telephone interview, Applicants' representatives faxed a set of proposed amended claims to the Examiner for discussion during the interview.

The proposed amended claims (which are identical to the claims filed herein) included independent claims 1 and 7.

Claim 1 recites a method of packaging a semiconductor device including (1) applying an insulative material including insulative beads across only a portion of at least two of a plurality of conductors providing interconnection between elements in the semiconductor device, and (2) encapsulating the conductors and elements, thereby packaging the semiconductor device.

Claim 7 recites a method of packaging a semiconductor device including (1) applying a solid insulator having an adhesive backing across only a portion of a plurality of conductors such that the adhesive backing is in contact with the portion of a plurality of conductors and not in contact with elements of the semiconductor device electrically connected by the plurality of conductors, and (2) encapsulating the conductors and elements, thereby packaging the semiconductor device.

As discussed during the telephone interview, none of (1) Shimanuki, (2) U.S. Patent Application Publication 2003/027918, (3) U.S. Patent No. 6,395,807, and (4) GB Patent No. 2,279,944 disclose the features of amended claims 1 or 7. A brief summary of the discussion regarding each of these four references is provided below.

Shimanuki does not disclose "applying an insulative material including insulative beads across only a portion of at least two of a plurality of conductors" (as in amended claim 1), nor does Shimanuki disclose "applying a solid insulator having an adhesive backing across only a portion of a plurality of conductors such that the adhesive backing is in contact with the portion of a plurality of conductors and not in contact with elements of the semiconductor device electrically connected by the plurality of conductors" (as in amended claim 7). In Shimanuki element 30 (shown in drawing 18) is heated to be disposed on semiconductor chip 5. In contrast, claim 7 recites that the solid insulator is applied such that it is not in contact with elements (e.g., a semiconductor chip or die) of the semiconductor device electrically connected by the plurality of conductors.

In U.S. Patent Application Publication 2003/027918 a semiconductor device is sealed with a filler containing spherical fused silica and which may contain metal impurities having a particle size of not larger than 53 μm (See Abstract). U.S. Patent Application Publication 2003/027918 neither discloses nor suggests, however, "applying an insulative material including insulative beads across only a portion of at least two of a plurality of conductors providing interconnection between elements in the semiconductor device" as recited in

amended claim 1. U.S. Patent Application Publication 2003/027918 teaches away from such a feature because the metal impurities in the filler could undesirably result in short-circuiting of a plurality of conductors if applied thereto.

In U.S. Patent No. 6,395,807 spherical silica is used as a filler for a resin sealing composition for a gap between an IC chip and a substrate, such as a gap in BGA and flip chip type devices (See Abstract and column 1, lines 28-36). U.S. Patent No. 6,395,807 neither discloses nor suggests, however, "applying an insulative material including insulative beads across only a portion of at least two of a plurality of conductors providing interconnection between elements in the semiconductor device" as recited in amended claim 1.

In GB Patent No. 2,279,944 spherical silica is used as a filler in a resin composition for encapsulating integrated circuits (See summary in paragraph 57). Claim 1 of the present application includes a step of "encapsulating the conductors and elements" to package the semiconductor device; however, applicants' invention as recited in claim 1 also includes a step of "applying an insulative material including insulative beads across only a portion of at least two of a plurality of conductors providing interconnection between elements in the semiconductor device." GB Patent No. 2,279,944 neither discloses nor suggests such a feature. Applicants have found that by applying the insulative material including insulative beads before the encapsulation process, the conductors are less likely to short circuit during the encapsulation process.

During the interview, it was agreed that, subject to a further search to be conducted by the Examiner, independent claims 1 and 7 (as well as their respective dependent claims) are patentably distinct from the art of record.

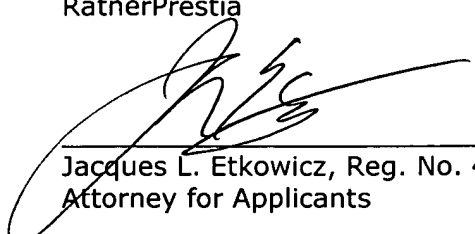
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Thus, subject to the results of the further search by the Examiner, allowance of the present application is respectfully requested.

Respectfully submitted,

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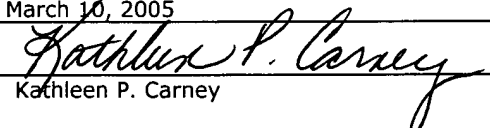
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